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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,095	06/16/2007	Takahiko Murata	067471-0119	1260

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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,095	MURATA ET AL.	
	Examiner	Art Unit	
	YOGESH K. AGGARWAL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :04/13/2009,07/11/2007,05/25/2007,06/16/2006.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 33-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Glenn et al. (US Patent # 6,266,197).

[Claim 33]

A solid-state imaging apparatus (figures 1 and 2) being one of pieces diced from an assembly, the solid-state imaging apparatus comprising:

a light-receiving chip (106) having a plurality of light-receiving cells arranged either one dimensionally or two dimensionally on one main surface of a base substrate, the main surface being made up of a light-receiving area (110) on which the light-receiving cells are arranged and a periphery area surrounding the light-receiving area (col. 9 lines 48-60, col. 10 lines 1-6); and

a transparent protection plate (120), at least a part thereof (122) that corresponds to the light-receiving area being transparent (col. 11 lines 4-11), wherein

the transparent protection plate has a skirt portion (124, molded part) at a periphery thereof (col. 7 lines 17-21, figures 1 and 2),

the skirt portion is positioned on the periphery area of the main surface thereby forming a space between the light-receiving cells and the transparent protection plate (col. 7 lines 17-21, figures 1 and 2), and

the assembly is comprised of two layers (figure 1 shows two layers), the two layers being a sheet of transparent protection plates (120) and a semiconductor wafer of light-receiving chips (102) that are attached to each other such that each transparent protection plate is combined with a corresponding light- receiving chip, and the diced pieces have such diced edges that result by cutting the two layers simultaneously (col. 1 lines 1-65).

[Claim 34]

The solid-state imaging apparatus of Claim 33, wherein the skirt portion is formed by plating metal on the periphery of the transparent protection plate that is a flat plate made of glass or resin.

[Claim 35]

The solid-state imaging apparatus of Claim 33, wherein the transparent protection plate (124) is a flat plate made of resin (col. 13 lines 53-col. 14 line 5), and the skirt portion is formed by pressing the flat resin plate.

[Claim 36]

A solid-state imaging apparatus (figures 1 and 2) being one of pieces diced from an assembly, the solid-state imaging apparatus comprising:

a light-receiving chip (106) having a plurality of light-receiving cells arranged either one dimensionally or two dimensionally on one main surface of a base substrate, the main surface being made up of a light-receiving area (110) on which the light-receiving cells are arranged and a periphery area surrounding the light-receiving area (col. 9 lines 48-60, col. 10 lines 1-6); and a transparent protection plate (120), at least a part thereof (122) that corresponds to the light-receiving area being transparent (col. 11 lines 4-11), wherein,

the light-receiving chip has, on the periphery area of the main surface, a rib portion having a loop shape (120),

the rib portion is attached onto a periphery of the transparent protection plate thereby forming a space between the light-receiving cells and the transparent protection plate (See figure 1 and 2), and

the assembly is comprised of two layers (figure 1 shows two layers), the two layers being a sheet of transparent protection plates (120) and a semiconductor wafer of light-receiving chips (102) that are attached to each other such that each transparent protection plate is combined with a corresponding light- receiving chip, and the diced pieces have such diced edges that result by cutting the two layers simultaneously (col. 1 lines 1-65)

[Claim 37]

The solid-state imaging apparatus of Claim 36, wherein the rib portion is an insulator made of a material for protective foil (col. 11 lines 56-col. 12 line 9, resin is an insulator).

[Claim 38]

A solid-state imaging apparatus (figures 1 and 2) being one of pieces diced from an assembly, the solid-state imaging apparatus comprising:

a light-receiving chip (106) having a plurality of light-receiving cells arranged either one dimensionally or two dimensionally on one main surface of a base substrate, the main surface being made up of a light-receiving area (110) on which the light-receiving cells are arranged and a periphery area surrounding the light-receiving area (col. 9 lines 48-60, col. 10 lines 1-6); wherein, a plurality of electrodes (bond pads 112) being provided outside the light- receiving area (figures 1 and 2); and

a transparent protection plate (120), at least a part thereof (122) that corresponds to the light-receiving area being transparent (col. 11 lines 4-11), wherein

the transparent protection plate includes: a plurality of terminal pads (104) formed on the other main surface that is different from the main surface,

a plurality of holes (215) are provided through the transparent protection plate, each hole electrically connecting one of the electrodes with a corresponding one of the terminal pads (see figure 2), and

the assembly is comprised of two layers (figure 1 shows two layers), the two layers being a sheet of transparent protection plates (120) and a semiconductor wafer of light-receiving chips (102) that are attached to each other such that each transparent protection plate is combined with a corresponding light- receiving chip, and the diced pieces have such diced edges that result by cutting the two layers simultaneously (col. 1 lines 1-65).

[Claim 39]

The solid-state imaging apparatus of Claim 38, wherein a plurality of holes are provided through the translucent protection plate (see 215 and 215A), and conductive foil is attached to a side wall of each of the holes (col. 15 line 60-col. 16 line 20).

[Claim 40]

The solid-state imaging apparatus of Claim 38, wherein a plurality of holes are provided through the translucent protection plate, and each of the holes is filled with a conductive material (col. 15 line 60-col. 16 line 20).

[Claim 41]

A solid-state imaging apparatus (figures 1 and 2) comprising:

a light-receiving chip (106) having a plurality of light-receiving cells arranged either one dimensionally or two dimensionally on one main surface of a base substrate, the main surface being made up of a light-receiving area (110) on which the light-receiving cells are arranged and a periphery area surrounding the light-receiving area (col. 9 lines 48-60, col. 10 lines 1-6); and a plurality of electrodes (bond pads 112) being provided outside the light- receiving area (figures 1 and 2); and

a transparent protection plate (120), at least a part thereof (122) that corresponds to the light-receiving area being transparent (col. 11 lines 4-11), wherein

the transparent protection plate includes: a plurality of terminal pads (104) formed on the other main surface that is different from the main surface,

and a plurality of conductive foils (215A) that are insulated from each other, each conductive foil electrically connecting one of the electrodes with a corresponding one of the terminal pads, and being attached to the main surface, a corresponding side surface, and the other main surface of the transparent protection plate (col. 10 lines 26-44).

[Claim 42]

The solid-state imaging apparatus of Claim 36, wherein the rib portion is produced on the periphery area of the main surface, by a semiconductor producing process (col. 11 line 57-col. 12 line 9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH K. AGGARWAL whose telephone number is (571)272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yogesh K Aggarwal/
Examiner, Art Unit 2622